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09/816,004	03/22/2001	Masakazu Suzuoki	SCEI 3.0-054	5183

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EXAMINER	
MANIWANG, JOSEPH R	
ART UNIT	**PAPER NUMBER**
2144	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,004	SUZUOKI ET AL.	
	Examiner	Art Unit	
	Joseph R. Maniwang	2144	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 8-17 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. "A computer readable medium for storing a software cell for transmission over a computer network, said computer network comprising a plurality of processors, said software cell comprising: a program...; data...; and a global identification..." is non-statutory, since it is not tangibly embodied in a manner so as to be executable, as the only hardware is in an intended use statement. This is true even if the recited "program", "data", and "global identification" includes hardware, since it is the intent of the execution of the system and not the system itself that includes such hardware.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Bernstein et al. (U.S. Pat. No. 6,668,317), hereinafter referred to as Bernstein.

5. Regarding claim 1, Bernstein disclosed a method and system comprising a plurality of processors connected to said network (see column 2, lines 48-51), each of said processors comprising a plurality of first processing units having the same instruction set architecture and a second processing unit for controlling said first processing units (see column 2, lines 56-67; column 3, lines 16-23), said first processing units being operable to process software cells comprising a program compatible with said instruction set architecture (see column 1, lines 48-50), data associated with said program (see column 3, lines 59-61) and an identification number uniquely identifying said software cell among all of said software cells being transmitted over said network (see column 3, lines 45-65).

6. Regarding claim 2, Bernstein disclosed the method and system wherein said second processing unit controls said first processing units by determining the programs of said software cells processed by said first processing units (see column 3, lines 45-59).

7. Regarding claim 3, Bernstein disclosed the method and system wherein each said first processing unit includes a local memory exclusively associated with said first processing unit and said first processing unit processes said programs from said local memory (see column 3, lines 37-44).

8. Regarding claim 4, Bernstein disclosed the method and system wherein each said processor further includes a main memory (see column 5, lines 36-45), said main

memory including a plurality of banks (see column 5, lines 46-59), each said bank including a plurality of blocks (column 5, lines 56-59), each said block being the lowest addressable unit of said main memory and having an associated memory space in said main memory for storing information regarding the status of data stored in said block (see column 19, lines 17-51), an identification for a first processing unit and an address of a local memory associated with said first processing unit (see column 19, lines 17-19).

9. Regarding claim 5, Bernstein disclosed the method and system wherein said first processing units comprise means for using said associated memory spaces to synchronize said first processing units' reading of data from, and writing of data to, said blocks (see column 4, lines 6-15).

10. Regarding claim 6, Bernstein disclosed the method and system wherein each of said processors further comprises a direct memory access controller (see column 3, lines 42-44).

11. Regarding claim 7, Bernstein disclosed the method and system wherein each said first processing unit is operable to issue a synchronize read command to read data from said main memory to a local memory associated with said first processing unit and to issue a synchronize write command to write data from said local memory to said main memory (see column 5, lines 46-51).

12. Regarding claim 18, Bernstein disclosed a method and system comprising a computer network comprising a plurality of processors (see column 2, lines 48-51); and a plurality of software cells configured for transmission over the computer network, each

of the software cells comprising a program for processing by one or more of said processors (see column 1, lines 48-50); data associated with said programs (see column 3, lines 59-61); and a global identification uniquely identifying said software cell among all software cells being transmitted over said network (see column 3, lines 45-65).

13. Regarding claim 19, Bernstein disclosed the method and system wherein each said software cell further comprises information for routing said software cell over said network (see column 4, lines 16-30).

14. Regarding claim 20, Bernstein disclosed the method and system wherein said information includes an identification for one of said plurality of processors, said one processor being the processor to which said software cell is to be transmitted for processing (see column 19, lines 17-19).

15. Regarding claim 21, Bernstein disclosed the method and system wherein said identification includes an internet protocol address (see column 4, lines 16-30).

16. Regarding claim 22, Bernstein disclosed the method and system wherein said information includes an identification for one of said plurality of processors, said one processor being the processor from which said software cell originates (see column 4, lines 31-39).

17. Regarding claim 23, Bernstein disclosed the method and system wherein said information includes an identification for one of said plurality of processors, said one processor being the processor to which information regarding the processing of said software cell is to be transmitted (see column 19, lines 52-61).

18. Regarding claim 24, Bernstein disclosed the method and system wherein each said software cell further comprises information providing a plurality of direct memory access commands for one of said processors (see column 3, lines 42-44).

19. Regarding claim 25, Bernstein disclosed the method and system wherein said information comprises a virtual identification for said one processor and addresses of a memory associated with said one processor for implementing said direct memory access commands (see column 19, lines 17-46).

20. Regarding claim 26, Bernstein disclosed the method and system wherein said global identification is based upon the identity of one of said processors, said one processor being a processor creating said software cell, and upon the time and date of said creating (see column 19, lines 52-61).

21. Regarding claim 27, Bernstein disclosed the method and system wherein said global identification is based upon the identity of one of said processors, said one processor being a processor transmitting said software cell, and upon the time and date of said transmitting (see column 19, lines 52-61).

22. Regarding claim 28, Bernstein disclosed a method and system comprising storing in said main memory said programs and said data associated with said programs (see column 17, lines 32-42); directing with said second processing unit any one of said first processing units to process one of said programs (see column 2, lines 61-67); directing with said second processing unit said memory controller to transfer said one program and data associated with said one program from said main memory to the local memory exclusively associated with said one first processing unit (see column

5, lines 18-35); instructing with said second processing unit said one first processing unit to initiate processing of said one program from said one first processing unit's local memory (see column 2, lines 61-67); and in response to said instructing, processing with said one first processing unit said one program and said data associated with said one pogrom from said local memory exclusively associated with said one first processing unit (see column 3, lines 16-23).

23. Regarding claim 29, Bernstein disclosed the method and system wherein said main memory is a dynamic random access memory (column 3, lines 24-36).

24. Regarding claim 30, Bernstein disclosed the method and system wherein said main memory includes a plurality of memory locations, each said memory location including a memory segment exclusively associated with said memory location (see column 5, lines 46-67).

25. Regarding claim 31, Bernstein disclosed the method and system further comprising storing in each said memory segment status information indicating the status of data stored in said memory segment's associated memory location, the identity of a first processing unit and a memory address (see column 5, lines 18-20; column 19, lines 17-46).

26. Regarding claim 32, Bernstein disclosed the method and system wherein said status information indicates the validity of said data stored in said memory segment's associated memory location (see column 19, lines 62-64), said identity indicates the identity of a particular one of said first processing units and said memory address

indicates a storage location within the local memory exclusively associated with said particular one first processing unit (see column 19, lines 17-51).

27. Regarding claim 33, Bernstein disclosed the method and system wherein each of said first processing units is a single instruction multiple data processor (see column 1, lines 24-25).

28. Regarding claim 34, Bernstein disclosed the method and system wherein each of said first processing units includes a set of registers, a plurality of floating points units, and one or more buses connecting said set of registers to said plurality of floating point units (see column 7, lines 15-53; column 8, lines 9-34).

29. Regarding claim 35, Bernstein disclosed the method and system wherein each of said first processing units further includes a plurality of integer units and one or more buses connecting said plurality of integer units to said set of registers (see column 8, lines 24-34).

30. Regarding claim 36, Bernstein disclosed the method and system wherein said computer processor comprises an optical interface, and further comprising converting electrical signals generated by said processor to optical signals for transmission from said computer processor over said waveguide and converting optical signals transmitted to said processor over said waveguide to electrical signals (see column 4, lines 16-30).

31. Regarding claim 37, Bernstein disclosed the method and system wherein each said local memory is a static random access memory (see column 3, lines 24-44).

32. Regarding claim 38, Bernstein disclosed the method and system wherein said computer processor further comprises a rendering engine, a frame buffer and a display

controller, and further comprising generating pixel data with said rendering engine, temporarily storing said pixel data in said frame buffer and converting with said display controller said pixel data to a video signal (see column 3, lines 10-15).

33. Regarding claim 39, Bernstein disclosed the method and system wherein the data associated with said one program includes a stack frame (see column 5, lines 18-35).

34. Regarding claim 40, Bernstein disclosed the method and system further comprising during said processing of said one program and said data associated with said one program, transferring with said memory controller, in response to an instruction to said memory controller from said one first processing unit, further data from said main memory to the local memory exclusively associated with said one first processing unit and thereafter processing said further data with said one first processing unit from said local memory exclusively associated with said one first processing unit (see column 18, lines 38-51).

35. Regarding claim 41, Bernstein disclosed the method and system wherein said main memory comprises a plurality of memory bank controllers and a cross-bar switch for providing a connection between each of said first processing units and said main memory (see column 5, lines 46-61).

36. Regarding claim 42, Bernstein disclosed the method and system further comprising prohibiting with said memory controller each said first processing unit from reading data from, or writing data to, any of said local memories with which said first processing unit is not exclusively associated (see column 5, lines 18-35).

37. Regarding claim 43, Bernstein disclosed the method and system further comprising following said processing of said one program and said data associated with said one program, transferring with said memory controller to said main memory, in response to an instruction to said memory controller from said one first processing unit, processed data resulting from said processing of said one program and said data associated with said one program (see column 7, lines 54-60).

38. Regarding claim 44, Bernstein disclosed the method and system wherein said memory controller is a direct memory access controller (see column 3, lines 42-44).

39. Regarding claim 45, Bernstein disclosed the method and system wherein said computer processor is connected to a network (see column 3, lines 45-65) and said one program is included within a software cell, said software cell containing a global identification uniquely identifying said software cell among all software cells transmitted over said network (see column 1, lines 48-50; column 3, lines 59-61; column 3, lines 45-65).

Response to Arguments

40. Applicant's arguments with respect to claims 1-45 have been considered but are moot in view of the new ground(s) of rejection.

41. Regarding claim 12, Examiner acknowledges Applicant's amendment to the claim in overcoming the objection. The objection has been withdrawn.

42. Regarding claims 18-27 previously rejected under 35 U.S.C. 101 as being drawn to non-statutory subject matter, Examiner acknowledges Applicant's amendment to the claims in overcoming the rejection. The rejection has been withdrawn.

43. Regarding claims 1-45 previously rejected under 35 U.S.C. 103(a) as being unpatentable over Jaffe et al. (U.S. Pat. No. 5,410,727), and further in view of Wilkinson et al. (U.S. Pat. No. 5,630,162), the rejection has been withdrawn and Applicant's traversal of the rejection is moot. Examiner submits that the claimed limitations are taught by the prior art as detailed above in the new grounds of rejection under 35 U.S.C. 102(e).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Corl, Jr. et al. (U.S. Pat. No. 6,799,207)

Wolrich et al. (U.S. Pat. App. Pub. 2002/0056037)

Wolrich et al. (U.S. Pat. No. 6,694,380)

Bernstein et al. (U.S. Pat. App. Pub. 2004/0205747)

Borkenhagen et al. (U.S. Pat. No. 6,567,839)

Alverson et al. (U.S. Pat. No. 6,840,818)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph R. Maniwang whose telephone number is (571) 272-3928. The examiner can normally be reached on Mon-Fri 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A. Wiley can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JM

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PRIMARY EXAMINER